IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	09/982,413
Applicant	:	Sohrab Kianian et al.
Filed	:	October 17, 2001
TC/A.U.	:	2826
Examiner	:	Scott R. Wilson
Title	:	SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH BURIED BIT-LINE AND VERTICAL WORD LINE TRANSISTOR (as amended)
Docket No.	:	2102397-992010
Customer No.	:	26379

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 1, 2003.

GRAY CARY WARE & FREIDENRICH Date: 12/01/03

By: Kathleen LaBrie

Kathleen LaBrie

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION OF JULY 31, 2003

Sir:

In response to the Office Action of July 31, 2003, please amend the above identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 13 of this paper.